

Figure 1

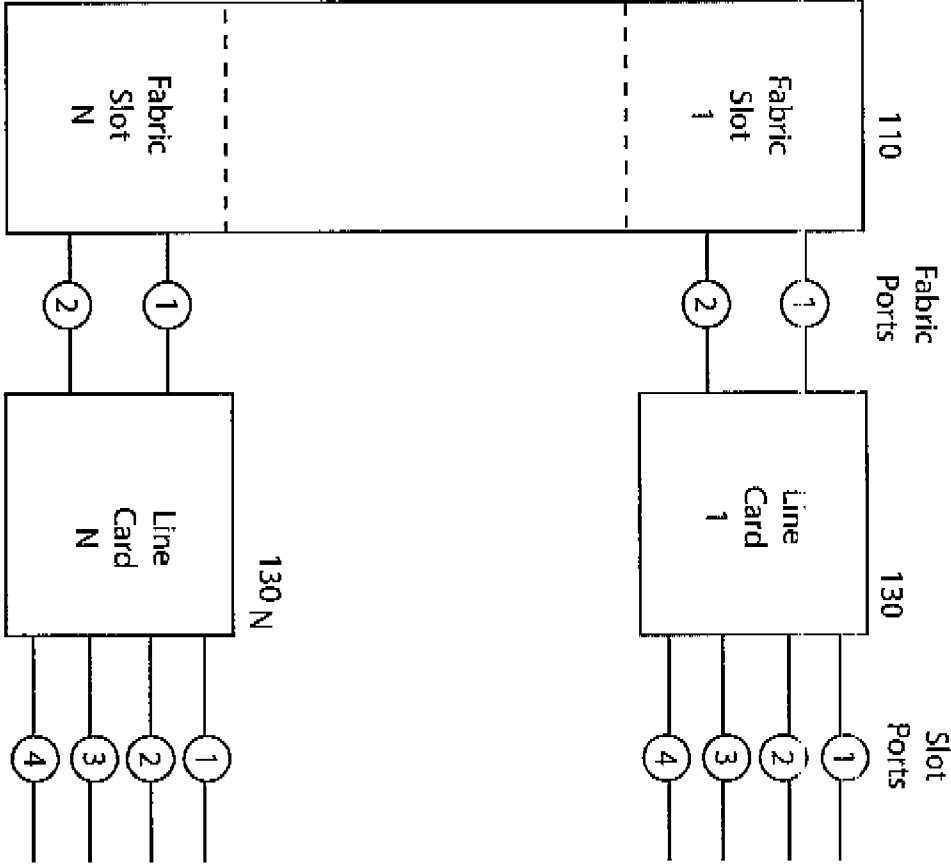


Figure 2

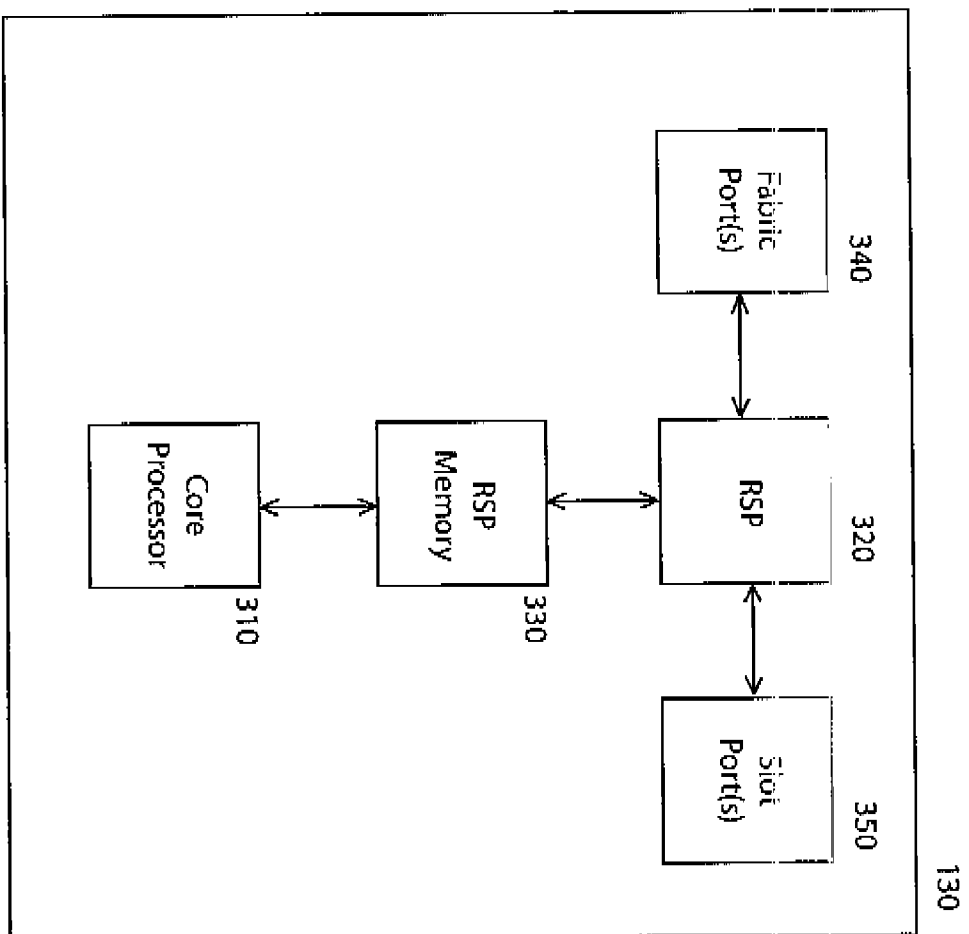


Figure 3

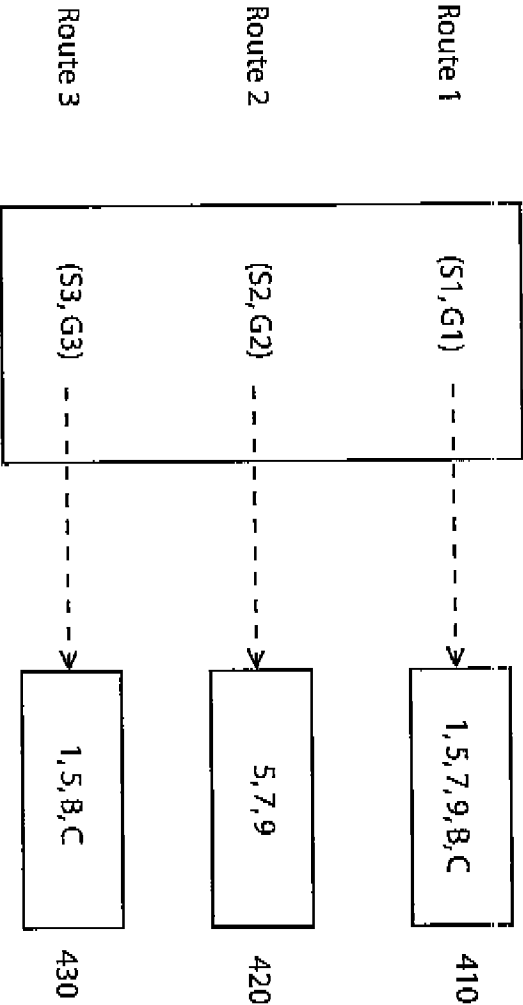


Figure 4A Main Routing Table

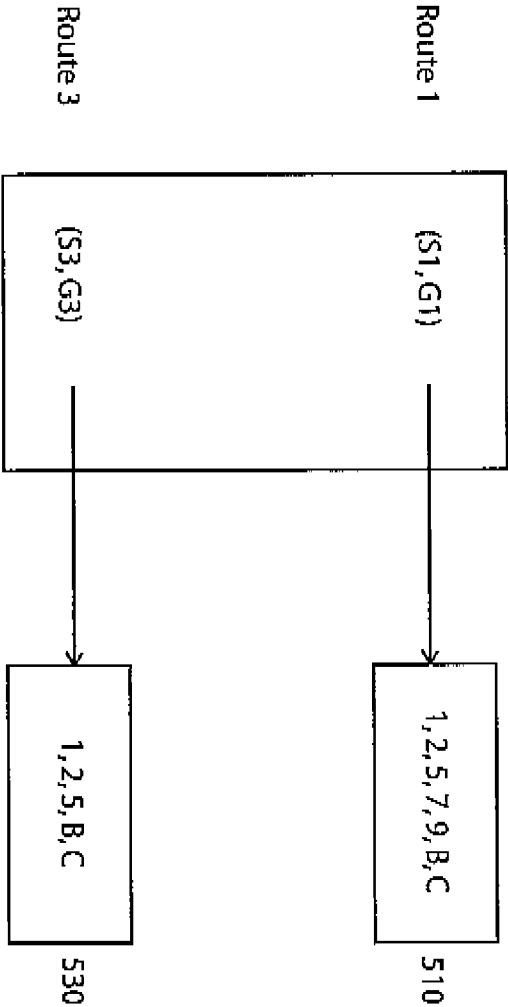


Figure 5A Bridged Routing Table [Slot 1, Slot 2]

[illegible]

Figure 5B

Bridged Routing Vector [Slot 1,Slot 2]

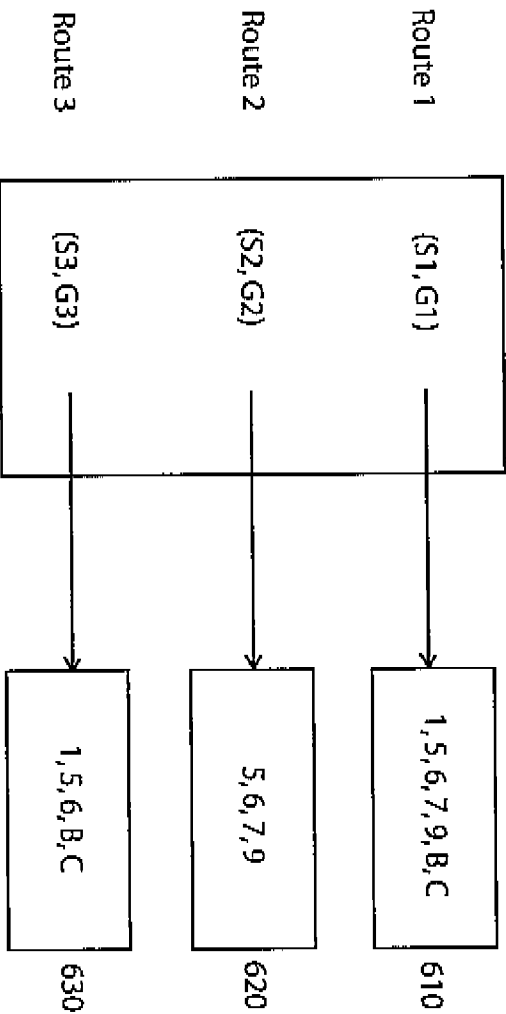


Figure 6A Bridged Routing Table [Slot 5, Slot 6]

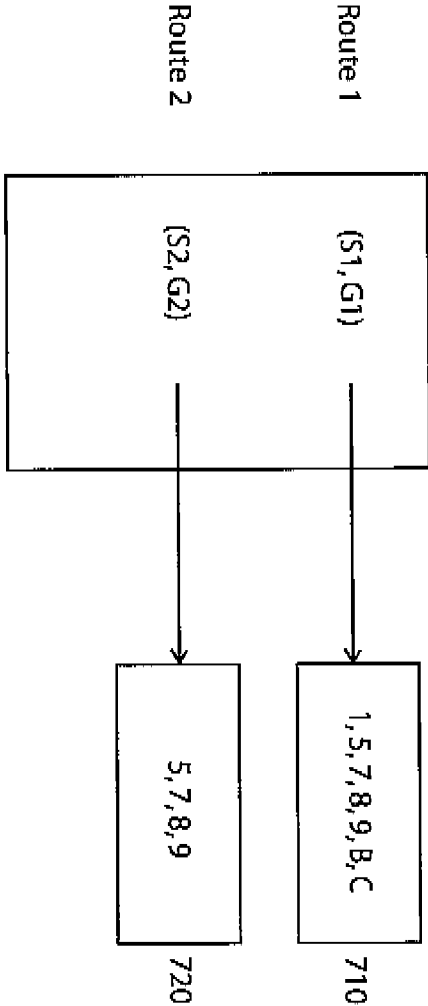


Figure 7A Bridged Routing Table [Slot 7, Slot 8]

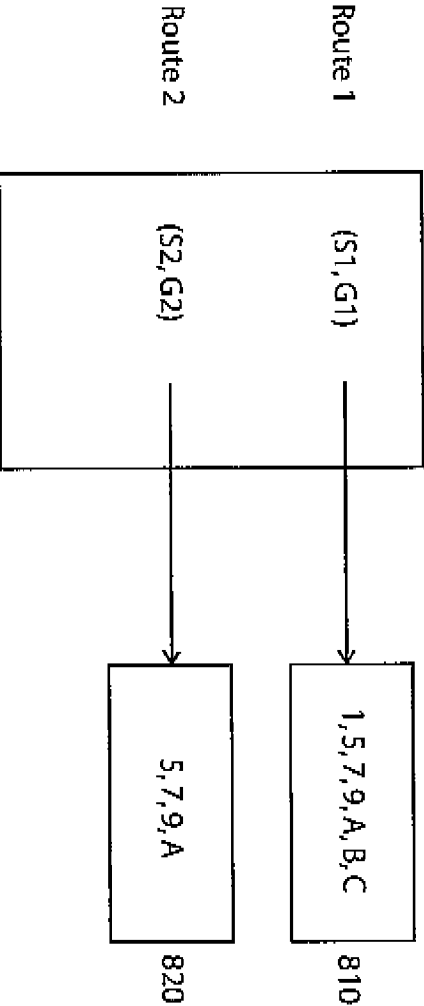


Figure 8A Bridged Routing Table [Slot 9, Slot A]

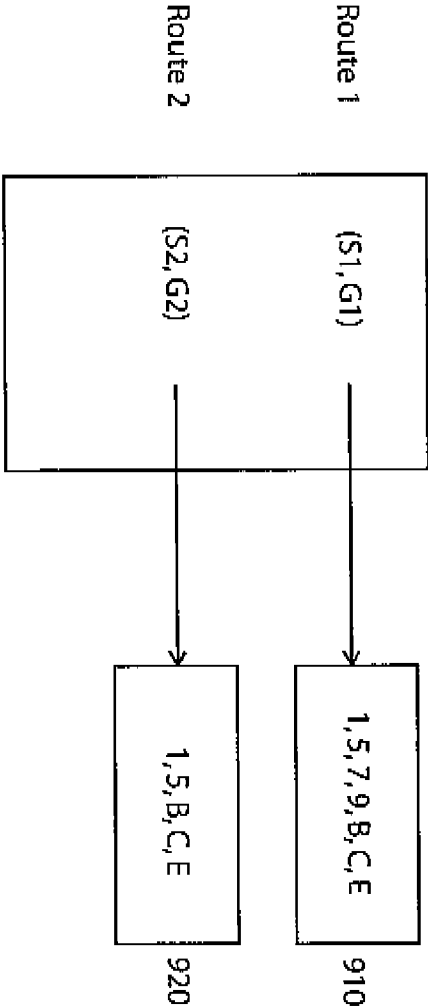


Figure 9A Bridged Routing Table [Slot 9, Slot E]















SLE	SLD	SLC	SLB	SLA	SL9	SL8	SL7	SL6	SL5	SL4	SL3	SL2	SL1
													

Figure 9B

Bridged Routing Vector [Slot 9, Slot E]

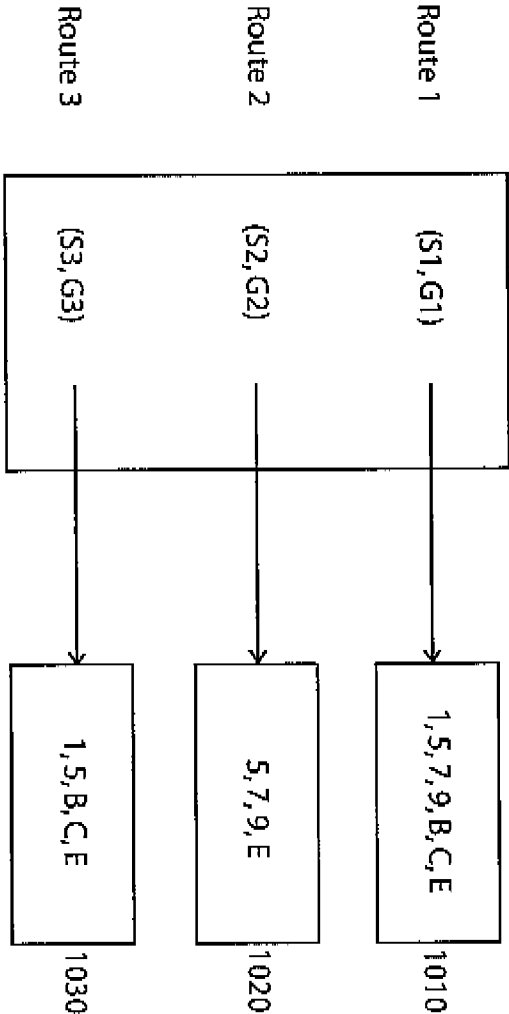


Figure 10A Bridged Routing Table [Slot 5, Slot E]

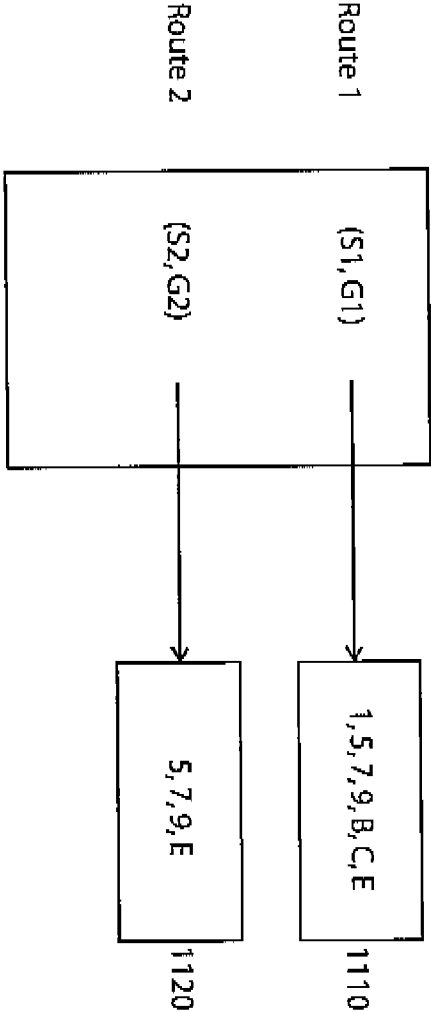


Figure 11A Bridged Routing Table [Slot 7, Slot E]















SLE	SLD	SLC	SLB	SLA	SL9	SL8	SL7	SL6	SL5	SL4	SL3	SL2	SL1
													

Figure 11B Bridged Routing Vector [Slot 7, Slot E] 1140

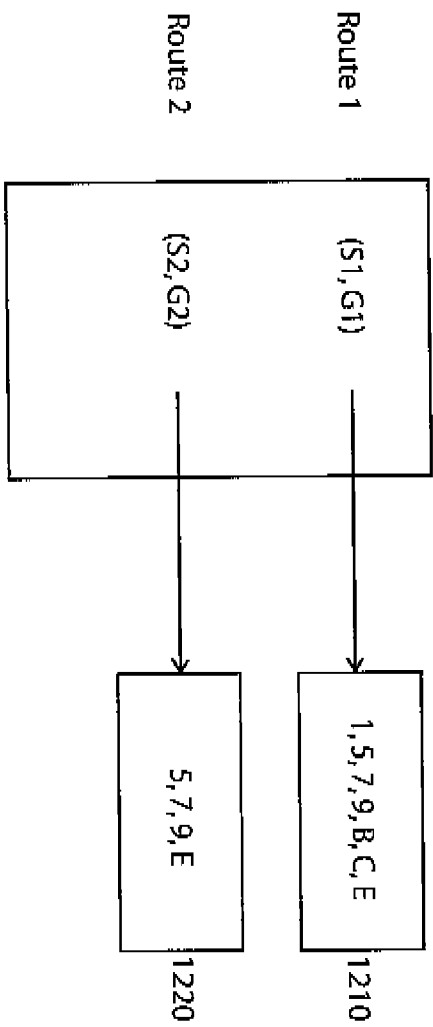


Figure 12A Bridged Routing Table [Slot 9, Slot E]

SLE	SLD	SLC	SLB	SLA	SL9	SL8	SL7	SL6	SL5	SL4	SL3	SL2	SL1

Figure 12B Bridged Routing Vector [Slot 9, Slot E]

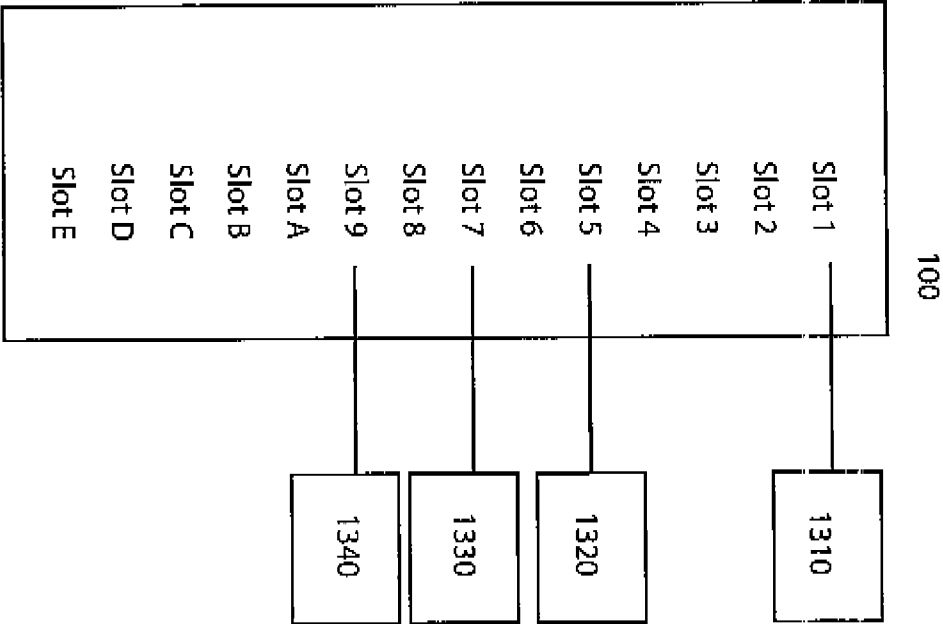


Figure 13 1300

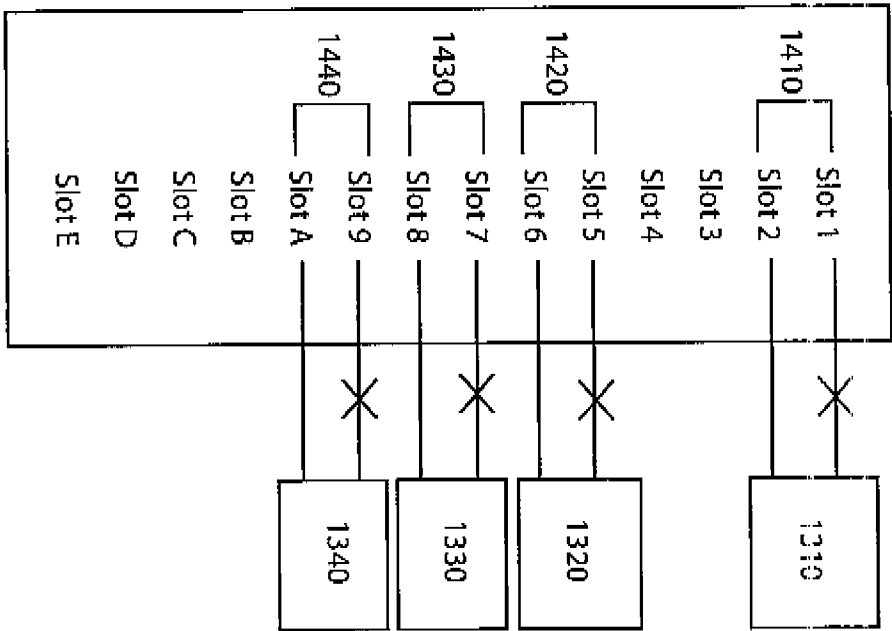


Figure 14 1400

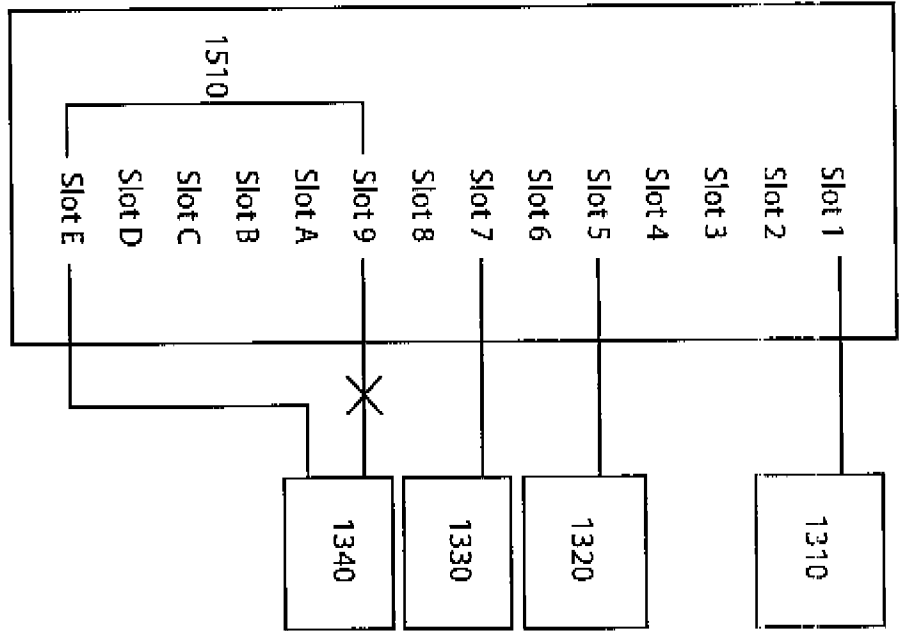


Figure 15 1500

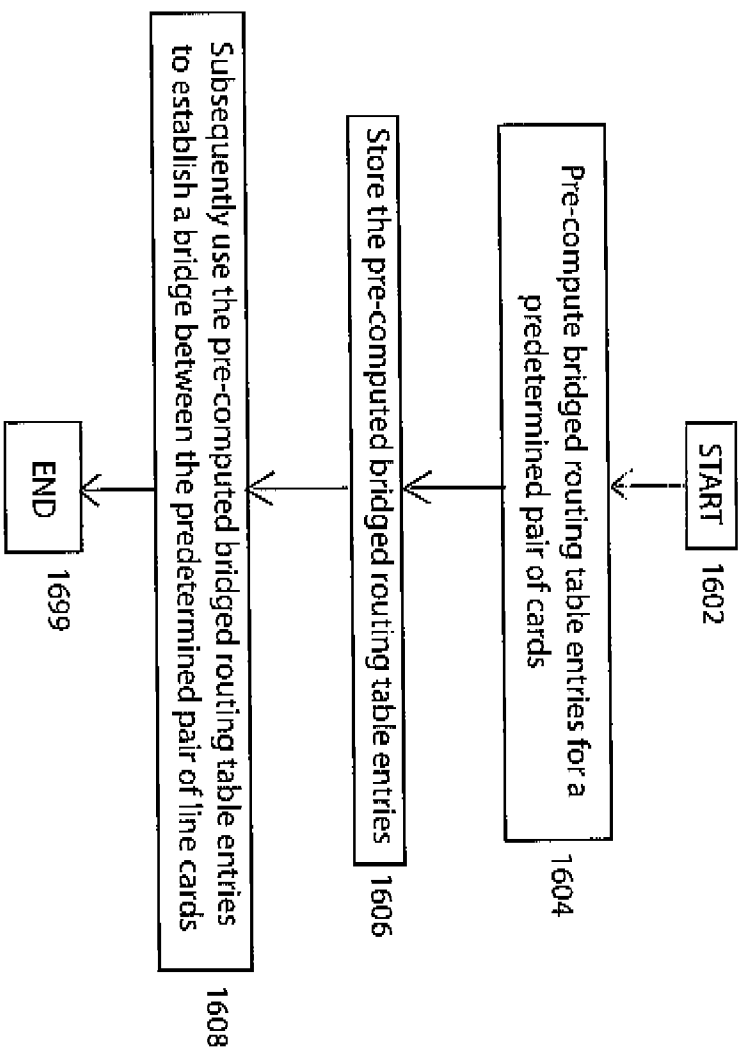


Figure 16 1600

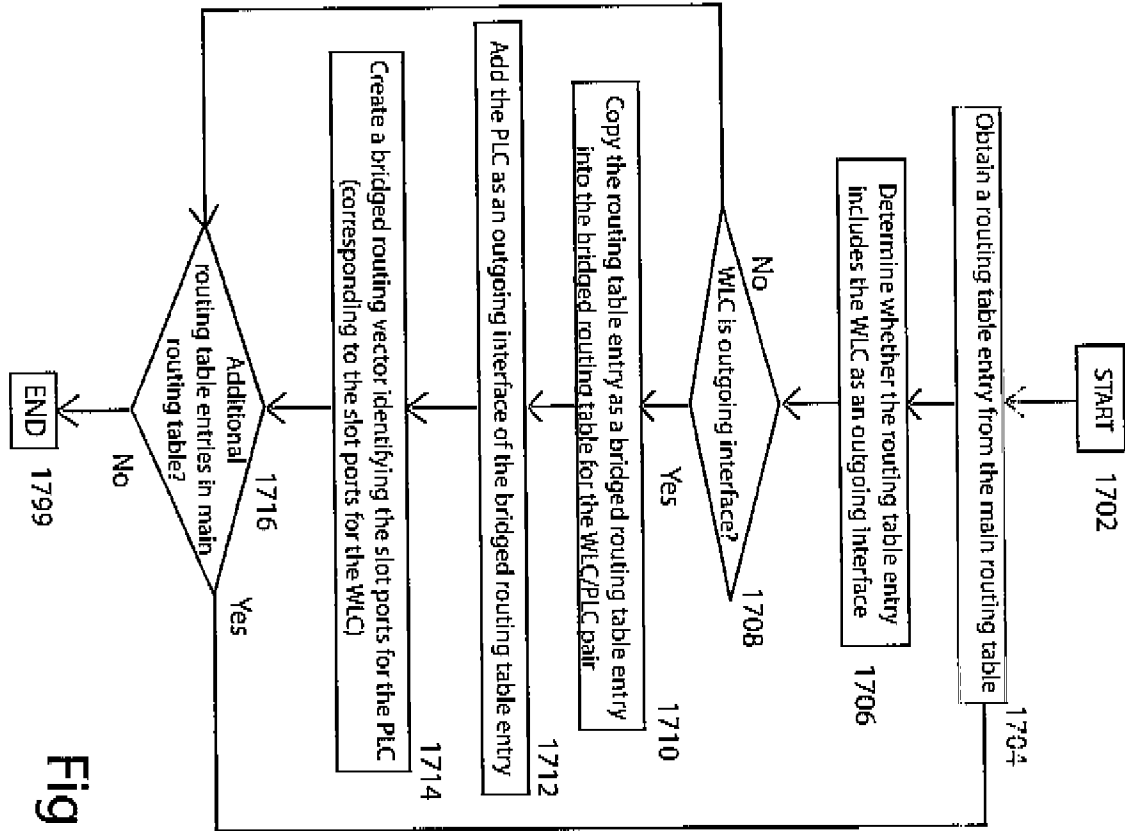


Figure 17 1700

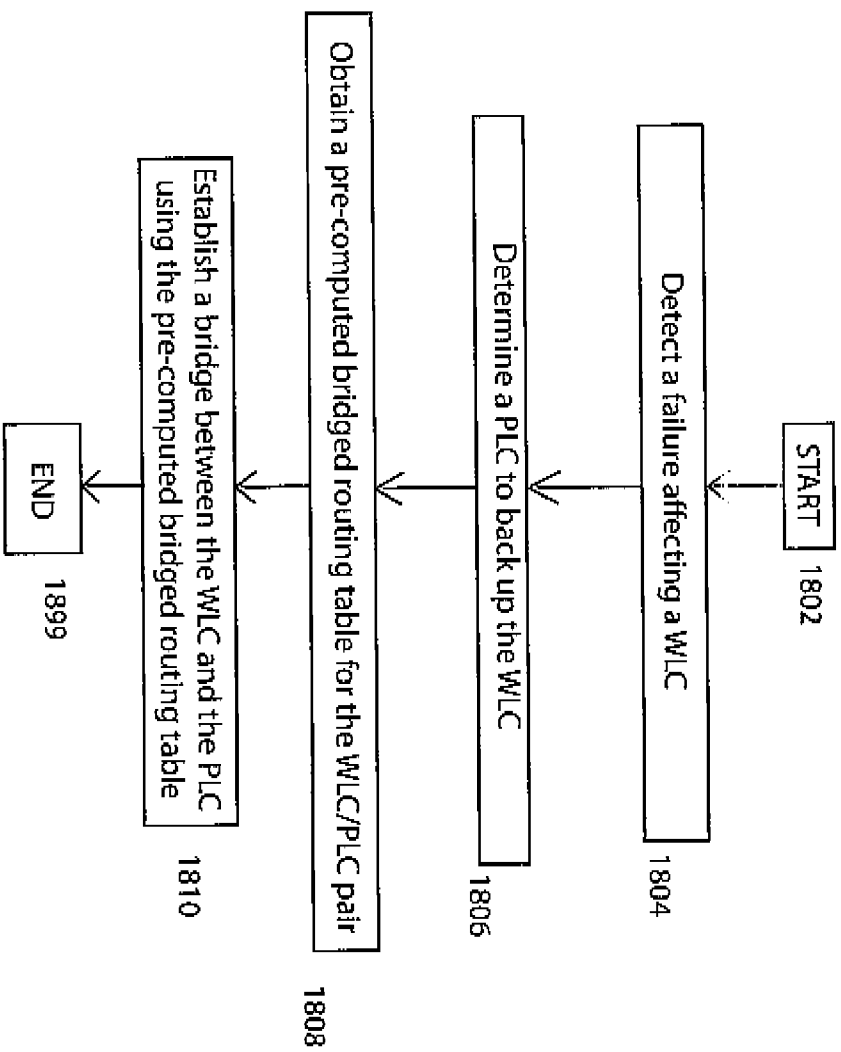


Figure 18 1800